Keynote Speech

Low-Power Testing for Low-Power Devices

PRESENTER

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Speaker Biography

Xiaoqing Wen r

eceived the B.E. degree in computer science and technology from Tsinghua University, Beijing, China in 1986, the M.E. degree in information engineering from Hiroshima University, Hiroshima, Japan in 1990, and the Ph.D. degree in applied physics from Osaka University, Osaka, Japan in 1993. From 1993 to 1997, he was an Assistant Professor at Akita University, Akita, Japan. He was a Visiting Researcher at University of Wisconsin – Madison, USA, from October 1995 to March 1996. He joined SynTest Technologies, Inc., Sunnyvale, USA, in 1998 and served as its Chief Technology Officer until 2003. In 2004, he joined Kyushu Institute of Technology, Iizuka, Japan, where he is currently a Professor. He served as the Chair of Department of Creative Informatics in 2008 and 2009.

Dr. Wen's research interests include test, testable design, and diagnosis of VLSI circuits. He currently holds 23 U.S. Patents and 5 Japan Patents in built-in self-test, test compression, and low-power test generation. He received the 2008 Society Best Paper Award from Institute of Electronics, Information and Communication Engineers – Information Systems Socisety for his pioneering work in low-capture power test generation. He co-authored and co-edited two books: VLSI Test Principles and Architectures: Design for Testability (San Francisco: Morgan Kaufmann, 2006) and Power-Aware Testing and Test Strategies for Low Power Devices (New York: Springer, 2009). He was the Program Committee Co-Chair of the Sixteenth IEEE Asian Test Symposium and the Eighth IEEE Workshop on RTL and High Level Testing. He is currently on numerous program committees, including IEEE/ACM Design Automation Conference (DAC), IEEE International Test Conference (ITC), Design, Automation, and Test in Europe (DATE), IEEE European Test Symposium (ETS), and IEEE Asian Test Symposium (ATS). He is the Associate Editor for the Information Processing Society Transactions on System LSI Design Methodology, Journal of Computer Science and Technology, and Journal of VLSI and Electronic System Design.

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Abstract

Low-power devices are indispensable for modern electronic applications, and numerous hardware/software techniques have been developed for drastically reducing functional power dissipation. However, the testing of such low-power devices has increasingly become a severe challenge, especially in at-speed scan testing where a transition is launched at the output of a flip-flop and the corresponding circuit response is captured by a flip-flop with a functional clock pulse. The reason is that most or all of the functional constraints with respect to circuit operations and clocking are ignored in at-speed scan testing, which may result in test power that is several times higher than functional power.

Excessive test power may cause die/package damage due to excessive heat as well as undue yield loss due to excessive power supply noise, as illustrated in Figure 1. As a result, it has become imperative to apply low-power testing to low-power devices. That is, low-power devices cannot be successfully realized without effective and efficient low-power test solutions.

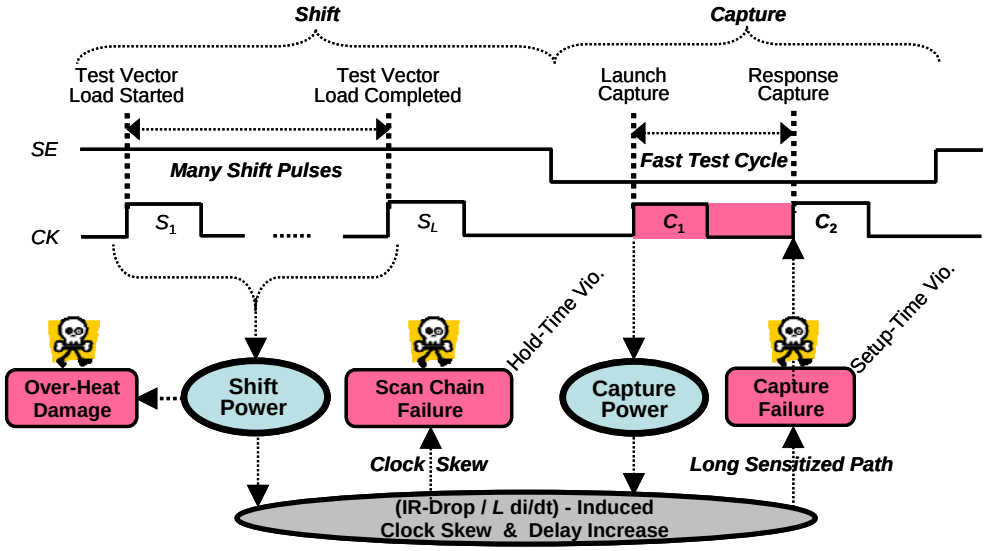

Figure 1. Impact of Test Power in LOC-Based At-Speed Scan Testing

This presentation first describes the basics of power dissipation in CMOS circuits. It goes on to highlight the difference between power dissipation in function mode and power dissipation in test mode, and lists the reasons why test power may become several times higher than functional power for low-power device. This presentation then describes the widely used clocking scheme for at-speed scan testing, namely launch-on-capture (LOC), and shows the different characteristics of shift power and capture power in LOC-based at-speed scan testing. Based on that, a general low-power testing strategy is outlined, featuring the use of design-for-test (DFT) for reducing shift power and the use of test data manipulation for reducing capture power. This presentation then provides a comprehensive review of the state-of-the-art techniques for reducing shift and capture power. Finally, future trends in the research and development for more advanced and sophisticated low-power testing solutions for low-power devices are discussed.